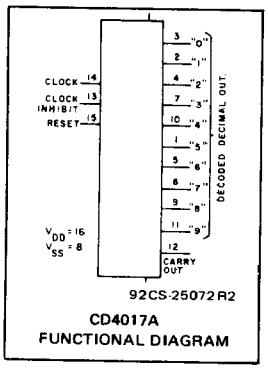
CMOS Decade Counter/Divider

Plus 10 Decoded Decimal Outputs

The RCA-CD4017A consists of a 5-stage Johnson decade counter and an output decoder which converts the Johnson binary code to a decimal number. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal.

The decade counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the clock INHIBIT signal is high. A high reset signal clears the decade counter to its zero count. Use of the Johnson decade counter configuration permits high speed operation, 2-input decimal decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 10 decoded outputs are normally low and go high only at their respective decimal time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT (C_{OUT}) signal completes one cycle every 10 clock input cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4017A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to + 85°C
DC SUPPLY-VOLTAGE RANGE (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

Features:

- Synchronous decade counter plus 10 decoded outputs
- Fully static operation
- Medium speed operation. . . . . 5 MHz (typ.) at $V_{DD} - V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range range)
- 1-V noise margin (full package-temperature range)

Applications:

- Decade counter/decimal decode display
- Frequency division
- Counter control/timers
- Divide by N counting
  N = 2 − 10 with one CD4017A and one one CD4001A
  N > 10 with multiple CD4017A's
- For further application information, see ICAN-6166 "CMOS MSI Counter and Register Design & Applications"

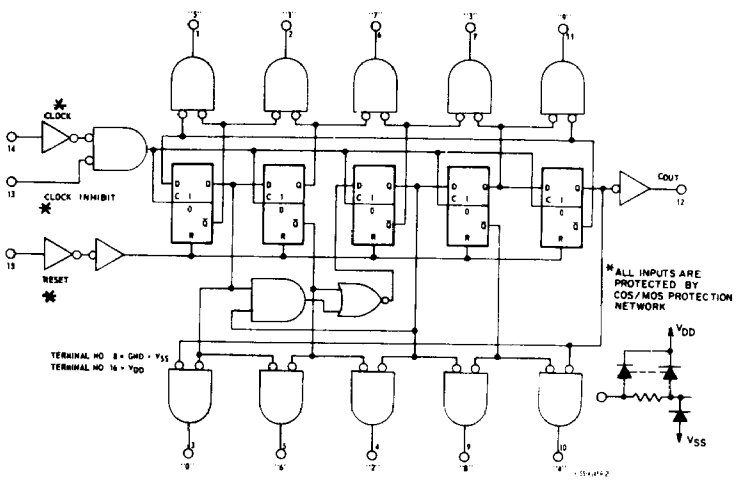


Fig. 1 – Logic diagram.

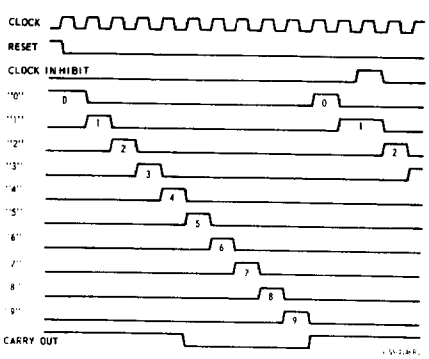


Fig. 2 – Timing diagram.

CD4017A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, K, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin Inputs Low V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_{DN} Min — Decoded Outputs	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	mA
	0.5	–	10	0.12	0.4	0.1	0.07	0.085	0.4	0.07	0.055	
I_{DN} Min — Carry Output	0.5	–	5	0.185	0.4	0.15	0.105	0.095	0.4	0.08	0.065	
	0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
P-Channel (Source) I_{DP} Min — Decoded Outputs	4.5	–	5	-0.0375	-0.075	-0.03	-0.021	-0.018	-0.075	-0.015	-0.012	
	9.5	–	10	-0.12	-0.2	-0.1	-0.07	-0.085	-0.2	-0.07	-0.055	
I_{DP} Min — Carry Output	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
	9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.24	-0.20	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

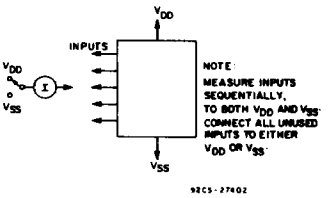


Fig. 10 – Input-leakage-current test circuit.

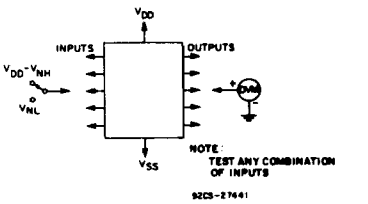


Fig. 11 – Noise-immunity test circuit.

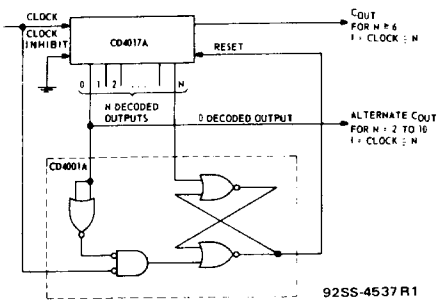


Fig. 12 – Divide by N counter ($N \leq 10$) with N decoded outputs.

When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001A) generates a reset pulse which clears the CD4017A to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next CD4017A counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017A. If the N^{th} decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	500 200	– –	700 300	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise or Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width, t_W	5 10	500 165	– –	830 250	– –	ns
Reset Removal Time	5 10	750 225	– –	1000 275	– –	ns

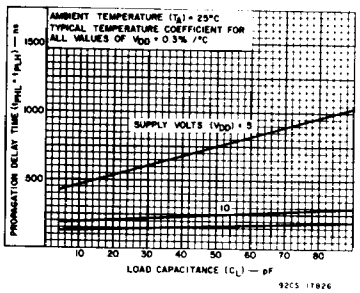


Fig. 3 – Typical propagation delay time vs. C_L for decoded outputs.

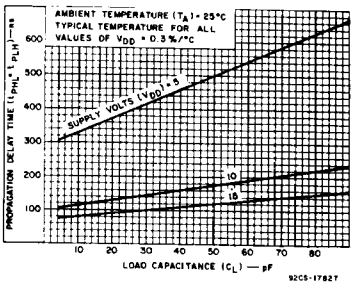


Fig. 4 – Typical propagation delay time vs. C_L for carry output.

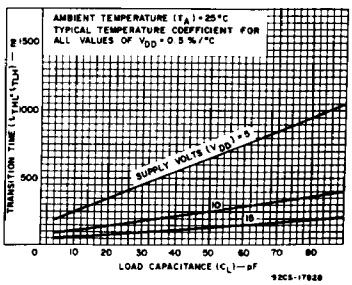


Fig. 5 – Typical transition time vs. C_L for decoded outputs.

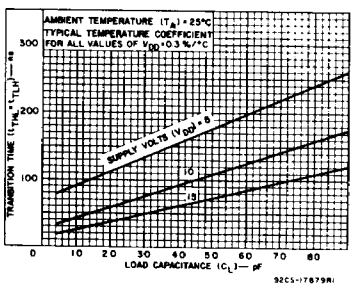


Fig. 6 – Typical transition time vs. C_L for carry output.

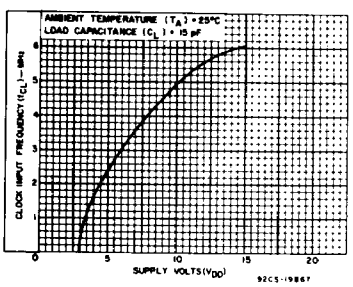


Fig. 7 – Typical clock input frequency vs. V_{DD}.

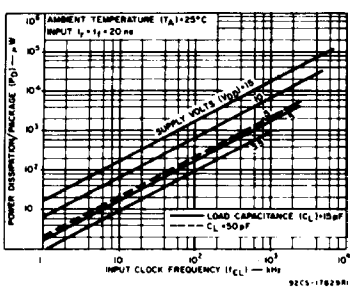
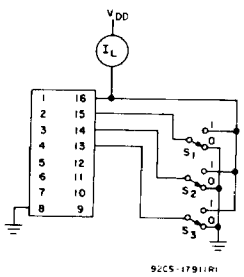


Fig. 8 – Typical dissipation characteristics.



Test performed with the following sequence of "1's and "0's" at each switch.

S_1	S_2	S_3	S_1	S_2	S_3
1	1	1	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
0	1	0	0	1	0
0	0	0	0	0	0
			0	1	0

Fig. 9 – Quiescent device current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, K, H PACKAGES			E PACKAGE			
		V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
CLOCKED OPERATION									
Propagation Delay Time; t_{PHL} t_{PLH}									
Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
Decode Out Lines		5	–	500	1200	–	500	1600	
		10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH}									
Carry Out Line		5	–	100	300	–	100	350	ns
		10	–	50	150	–	50	200	
Decode Out Lines		5	–	300	900	–	300	1200	
		10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}*		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2	5	–	
Minimum Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	170	–	100	250	
Clock Rise & Fall Time: t_rCL, t_fCL		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Minimum Clock Inhibit Set-Up Time, t_s		5	–	175	500	–	175	700	ns
		10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time; t_{PHL}									
To Carry Out Line		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Decode Out Lines		5	–	450	1200	–	450	1600	
		10	–	200	400	–	200	500	
Minimum Reset Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	165	–	100	250	
Minimum Reset Removal Time		5	–	300	750	–	300	1000	ns
		10	–	100	225	–	100	275	

*Measured with respect to carry output line